ACORN 80 x 25 VDU INTERFACE BOARD

UNIT DESCRIPTION

CONTENTS

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1. INTRODUCTION

1.1 GENERAL

The 80 x 25 VDU Interface Board provides the interface between a Microcomputer System, such as the Acorn System 5 and a monochrome Visual Display Unit (VDU). A block diagram of the VDU Interface Board is given on Figure 1.

The VDU Board receives characters to be displayed in 8 bit bytes on the Acorn Bus. The characters are stored in the 2048 (2K) byte Random Access Memory (RAM). The VDU Controller IC reads the characters to be displayed from the Character RAM into a Read Only Memory (ROM). The ROM is programmed to convert the characters from the code used in the System, i.e. American Standard Code for Information Interchange (ASCII), to a dot output of '1's and '0's. The ROM output is converted to a serial dot pattern which produces the required characters on the VDU screen.

The VDU Controller also provides the Horizontal Synchronization (HS) and Vertical Synchronization (VS) signals, which are combined with the dot output to generate the composite video signal to the VDU.

The VDU Board can be operated directly from the Acorn Bus 6502A 2MHz and 12MHz clock signals. Alternatively, an on-board clock circuit may be used to generate the clock signals from the Phase 2 (§2) clock in a 1MHz or 2MHz CPU system (e.g. 6809).

Address Selection Links on the VDU Board are provided to allow two possible Character RAM address locations, either Block 1 1000 to 17FF hexadecimal (hex) or Block F F000 to F7FF (hex). The VDU Controller addresses are 1840 and 1841 (hex) for System 5 or E840 and E841 (hex) for 6809. Note that addresses 1840 to 187F (hex) or E840 to E87F (hex) must be reserved for the VDU Board, since the addresses are not completely decoded.

The Character RAM may be accessed at any CPU §2 clock time by a Read or Write operation, without affecting the video output.

1.2 PRINCIPLES OF OPERATION

The characters to be displayed are written into the locations in the Character RAM that correspond to the display positions on the VDU screen. The Character RAM locations are addressed by the VDU Controller to obtain the characters during the Phase 1 (§1) CPU clock time. The characters are loaded into (or read from) the Character RAM locations during the Phase 2 (§2) clock time. The VDU Controller is used in the consecutive binary address mode. In this mode each character display location is identified by a binary number, starting with 0 in the top left hand display position, refer to Figure 2.

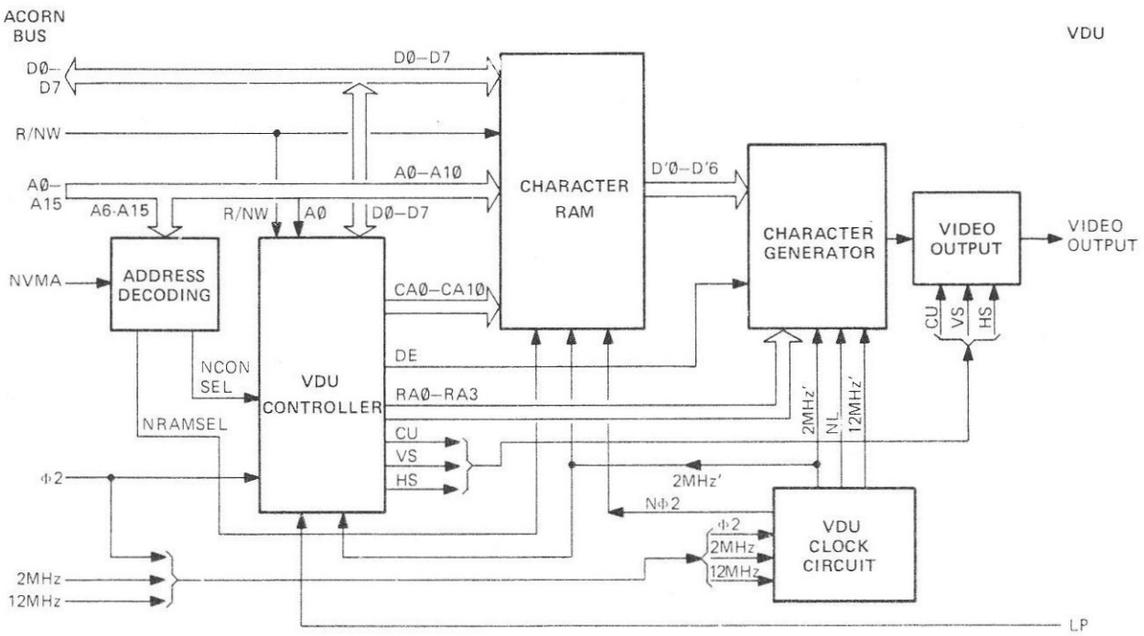

Figure 1. 80 x 25 VDU Interface Board Block Diagram

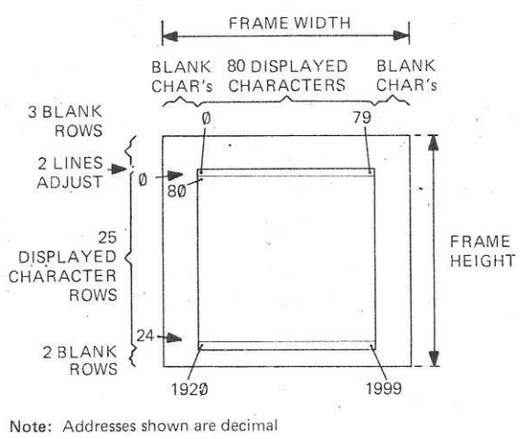

Figure 2. VDU Scan (1 Frame 50Hz)

The character timing and the number of scan lines per character row are programmable. The characters are displayed as a dot matrix on the VDU screen. Figure 3 shows an example of a letter 'H' displayed as a 5 x 8 dot matrix. A character time of 0.5µs with a dot clock of 12MHz is used to produce the five character dots plus the inter-character space. In the example, a scan of 10 lines per character row gives the 8 scan lines for the character, plus two inter-character scan lines for vertical spacing or the Cursor. The Cursor may be displayed as an underline or a character block. The Cursor is positioned by Writing the character number to the Cursor Position Register in the VDU Controller.

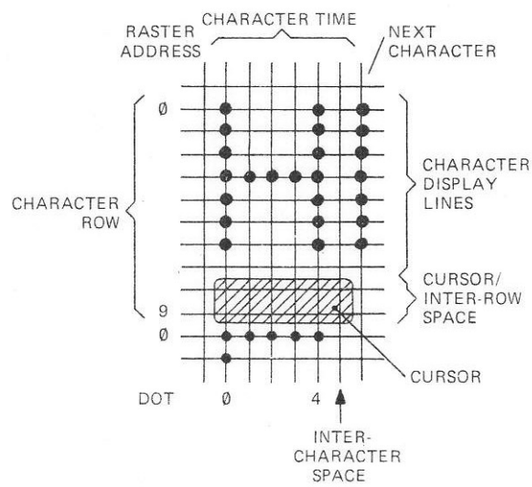

Figure 3. Character Dot Matrix

1.3 LEADING PARTICULARS

1.3.1 Mechanical

Construction : Single Eurocard printed circuit board.

Size : 100mm x 160mm

1.3.2 Power Supplies

+5V ± 5% at 450mA typically.

1.3.3 Connections

Pin connections are given in Section 4.

Connectors : Double sided edge connector to Acorn Bus, TTL signal levels are used, 0V to 0.4V = logic '0', >=+2. 4V = logic '1'.

5 way connector for ribbon cable to connector on the front panel. Composite video output at 1V into 75Ohm. Light Pen input, TTL.

2. CIRCUIT DESCRIPTION

Reference should be made to the circuit diagram, Figure 18 in conjunction with this description. The Character ROM and Link Location is given on Figure 4.

2.1 ADDRESS DECODING

The Acorn Bus address lines A6 to A15 are decoded by IC1 and IC2 to select the Character RAM or the VDU Controller, refer to Figure 5. The Valid Memory Address (NVMA) signal may be used for paging the VDU Board in the System memory; to use this facility the track link LK3 must be cut.

2.1.1 RAM Selection

The address lines A11 to A.15 are decoded by IC1 when it is enabled by either the NVMA signal low, or 0V via LK3. The address Block for the RAM is selected by Links LK9, LK10 and LK11, refer to Table 1. The VDU Board is supplied with the links in position A to give addresses in Block 1. To select addresses in Block E the links in position A must be removed and links soldered in position B.

The appropriate outputs of IC1 are similarly selected by the positions of LK12 and LK13. Outputs YO or Y6 generate signal NRAMSEL low to select the Character RAM. Outouts Y1 or Y3 enable IC2 to select the VDU Controller.

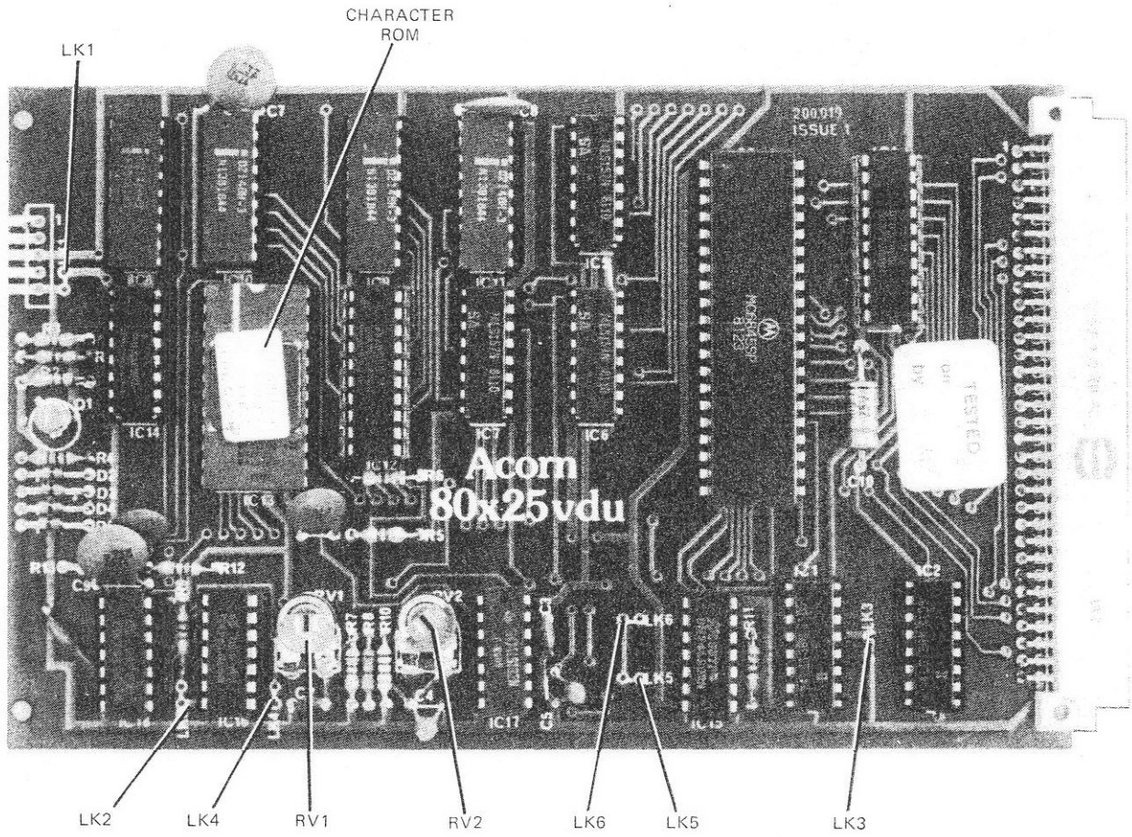

Figure 4. 80 x 25 VDU interface Board

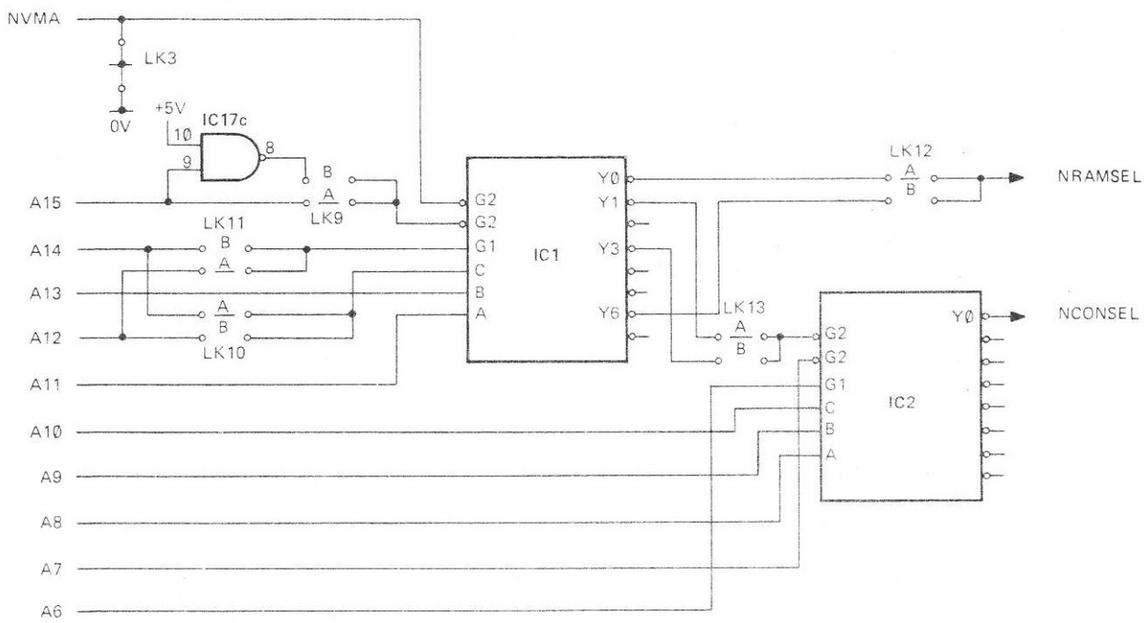

Figure 5. Address Decoding Circuit

Links	NVMA	A 15 14 13 12 11	IC1/Y Ø 1 3 6	Address (Hex)	Select
	1	X X X X X	1 1 1 1		
A	Ø	Ø Ø Ø 1 Ø	Ø 1 1 1	1Ø00-17FF	RAM
B	Ø	1 1 1 1 Ø	1 1 1 Ø	F000-F7FF	
A	Ø	Ø Ø Ø 1 1	1 Ø 1 1	1800-18FF	IC2
B	Ø	1 1 1 Ø 1	1 1 Ø 1	E800-E8FF	

(a) RAM Select

Links	IC1 Y1	IC1 Y3	A 1Ø	A 9	A 8	A 7	A 6	IC2 YØ	Address (Hex)
A	Ø	X	Ø	Ø	Ø	Ø	1	Ø	184Ø-187F
B	X	Ø	Ø	Ø	Ø	Ø	1	Ø	E84Ø-E87F

(b) VDU Controller Select

X = irrelevant

Table 1. VDU Board Address Decoding

2.1.2 VDU Controller Selection

The selected Y1 or Y3 output of IC1 enables IC2, which decodes Acorn Bus address lines A6—A10 to generate the NCONSEL signal low and select the VDU Controller for Read or Write operations. Note that the VDU Controller address is not fully decoded, so that any addresses in the range 1840 to 187F (hex) or E840 to E87F (hex) will select the Controller.

2.2 VDU CONTROLLER

The VDU Controller is a HD46505SP-2 IC operating under program control. The VDU Controller has 19 addressable Registers. The Acorn Bus address line A0 is used to select a Register when the Controller is selected. A Write operation to the Controller with a '0' on A0 selects the Address Register. The Register number on data bits D0—D4, will then determine which Register will be selected by a subsequent Read or Write operation to the VDU Controller, with A0 = '1'. Refer to Table 2 and paragraph 2.2.1 for the Registers and their functions.

The VDU Controller generates the VDU screen character positions as consecutive binary numbers on the Character Address lines CA0—CA10. The position of a character is completely defined by the address, refer to Figure 2. The display is organized into character rows, the Vert. Displayed Register specifies the number of rows, the Horiz. Displayed Register the number of characters (char.) per row to be dis-

SIGNAL R/NW	SIGNAL AØ	ADDRESS REG. BITS 4	3	2	1	Ø	REGISTER No.	REGISTER NAME	FUNCTION
Ø	Ø	—	—	—	—	—	AR	Address	Contains selected Register No.
Ø	1	Ø	Ø	Ø	Ø	Ø	RØ	Horiz. Total	No. of char./line — 1
Ø	1	Ø	Ø	Ø	Ø	1	R1	Horiz. Displayed	No. of char./line displayed
Ø	1	Ø	Ø	Ø	1	Ø	R2	HS Position	Start of HS (char. No. — 1)
Ø	1	Ø	Ø	Ø	1	1	R3	Sync Width	Sync pulse width DØ—D3 = Char. times (HS) D4—D7 = Scan lines (VS)
Ø	1	Ø	Ø	1	Ø	Ø	R4	Vert. Total	No. of char. rows/frame — 1
Ø	1	Ø	Ø	1	Ø	1	R5	Vert. Total Adjust.	No. of scan lines to complete frame
Ø	1	Ø	Ø	1	1	Ø	R6	Vert. Displayed	No. of char. rows displayed/frame
Ø	1	Ø	Ø	1	1	1	R7	VS Position	Start of VS (char. row No. — 1)
Ø	1	Ø	1	Ø	Ø	Ø	R8	Interlace & Skew	Select Interlace Mode
Ø	1	Ø	1	Ø	Ø	1	R9	Max. Taster Address	No. of scan lines/char. — 1
Ø	1	Ø	1	Ø	1	Ø	R1Ø	Cursor Start Raster	DØ—D4 = Cursor start (scan line No.) D5, D6 = Cursor Mode
Ø	1	Ø	1	Ø	1	1	R11	Cursor End Raster	Cursor end (scan line No.)
Ø/1	1	Ø	1	1	Ø	Ø	R12	Start Address (H)	Address of start of display (char. No.)
Ø/1	1	Ø	1	1	Ø	1	R13	Start Address (L)	
Ø/1	1	Ø	1	1	1	Ø	R14	Cursor (H)	Address of Cursor position (char. No.)
Ø/1	1	Ø	1	1	1	1	R15	Cursor (L)	
1	1	1	Ø	Ø	Ø	Ø	R16	Light Pen (H)	Address of Light Pen position (char. No.)
1	1	1	Ø	Ø	Ø	1	R17	Light Pen (L)	

Table 2. VDU Controller Registers

played. The 80 x 25 VDU Interface Board can display up to 2000 char., arranged as 25 rows with 80 char. in each row.

The number of scan lines per char. row is selected by program. The VDU Controller generates the scan line addresses on Raster Address lines RA0—RA3 for each char. row.

2.2.1 Register Functions

The functions of the VDU Controller Registers are as follows:

- ADDRESS (AR): Contains the vector number (hex) of the specified internal Control Register in bits 0-4. Accessed by a Write operation when A0 = '0'r
- HORIZ. TOTAL (R0): Contains the total number of char. in a row, minus one. (Determines HS frequency).
- HORIZ. DISPLAYED (R1): Contains the total number of char. to be displayed in a row, i.e. 80.
- HS POSITION (R2): Contains the number of the char. position in a row, minus one, at which the HS signal starts.
- SYNC WIDTH (R3): Divided into two parts, Bits 0-3 define length of HS signal in char. time units in hex (bits 0-3 = 0000 not valid). Bits 4-7 define length of VS signal as number of scan lines index (except, bits 4-7 = 0000 given 16 scan lines duration).
- VERT. TOTAL (R4): Total number of char. rows, minus one. Bit 7 not used.
- VERT. TOTAL ADJUST (R5): Contains the number of additional scan lines to complete scan field. Bits 5-7 not used.
- VERT. DISPLAYED (R6): Contains the total number of rows to be displayed on the VDU Screen. Bit 7 not used.
- VS POSITION (R7): Contains the number of the char. row, minus one, at which the VS signal starts. Bit 7 not used.
- INTERLACE & SKEW (R8): Selects the VDU Controller operating mode, refer to Figure 6.
- MAXIMUM RASTER ADDRESS (R9): Contains the total number of scan lines per char. row, including spacing, When Non-interlace' Mode or Interlace Sync Mode selected the number of scan lines per char, row, minus one, is required. For Interlace Sync and Video Mode the number of scan lines per char. row, minus two, is required. Bits 5-7 not used.
- CURSOR START RASTER (R10): Bits 0-4 contain the number of the first scan line of the Cursor in a char. row, Bit 7 nis not used. Bits 5 and 6 control the Cursor Mode as follows:

BIT 6	BIT 5	CURSOR MODE
0	0	No blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

NOTE: For Block Cursor set R10 to 0 and R11 to last char. scan line number.

— CURSOR END RASTER (R11): Bits 0-4 contain the number of the last scan line of a Cursor in a char. row. Bits 5-7 not used.

— START ADDRESS (R12, R13): A two byte Register that contains the char. number from which the display starts. When scrolling is required the address of the first char, in the top row to be displayed is loaded into R12 and R13. R12 bits 6 and 7 not used (00 when read).

— CURSOR POSITION (R14, R15): A two byte Register that contains the char. number at which the Cursor is to be displayed. R14 bits 6 and 7 not used *(00* when read).

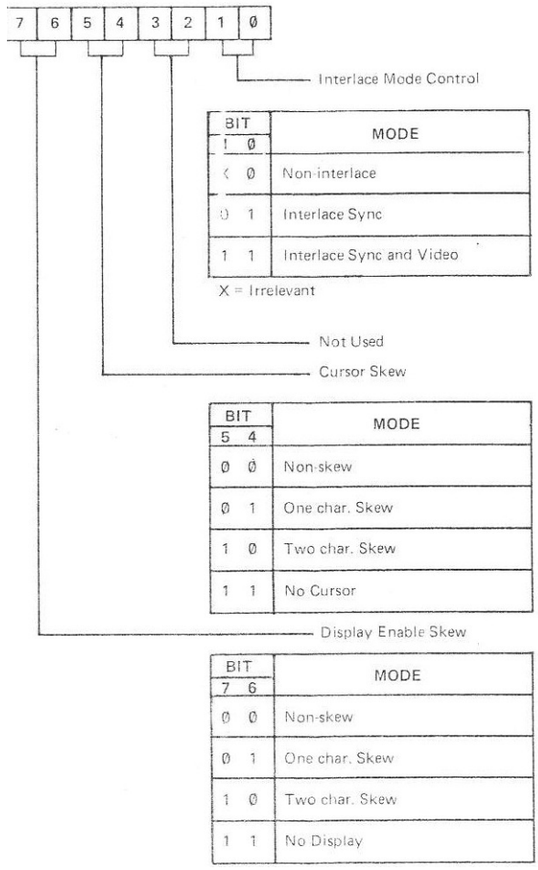

Figure 6. Interlace and Skew Register (R8) Bit Significance

- LIGHT PEN (R16, R17): A two byte Register that is loaded with the char. number, when a positive edge is detected on the LP input. R16 bits 6 and 7 are always 00. (Refer to para 2.2.5 for further details).

2.2.2 System Interface Signals

The following inputs and outputs are used to control the operation of the VDU Controller:

— §2: The CPU Phase 2 (§2) clock input controls the timing of data transfers between the System and the VDU Controller.

- R/NW: This signal input from the System selects the direction of data transfers.
- NCS: The Chip Select signal input is set low by the NCONSEL signal from the address decoder, when the VDU Controller address is detected.
- RS: The Register Select input is connected to address line A0. A '0' on A0 selects either the Address Register for a Write operation or the Status Register for a Read operation. When A0 is '1' the address in the Address Register determines which Register is accessed by the System.
- D0—D7: The Data input/output lines are enabled by a low on the NCS input. The lines are high impedance when NCS is high.

2.2.3 Video Interface Signals

The following inputs and outputs are used by the VDU Controller to control the video output from the VDU Board:

- HS: This signal generates the horizontal (lines) sync pulse to the Video Circuit. The timing of the signal is programmable, refer to para 2.2.1.
- VS: This signal generates the vertical (frame) sync pulse to the Video Circuit. The timing of the signal is programmable, refer to para 2.2.1.
- DE: The Display Enable (DE) signal is set high during the transmission of the display characters, refer to para 2.2.7.
- CU: The Cursor (CU) signal is set high when the character address corresponds to the Cursor address held in the Cursor Address Register. The Cursor may be either a block, or an underline, the mode of operation is selected by program.
- CK: The Clock (CK) input is driven by the 2MHz' clock, generated by the Clock Circuit, refer to para 2.3.1.

2.2.4 Memory Address Signals

The following memory address signals are used to select the display characters:

- CA0—CA10: The Character Address (CA) lines provide the binary addresses of the locations in the RAM, which contain the characters to be displayed.
- RA0—RA3: The Raster Address (RA) lines are used to select the appropriate dot output from the Character ROM on the current scan line to produce the characters read from the RAM location by CA0—CA10.

2.2.5 Light Pen

The Light Pen (LP) input stores the current character address in the Light Pen Register, when a positive edge is detected on the input. LK1 is used to connect the input to 0V when not used.

Since there is a two char. time delay between the output of a char. address from the VDU Controller and the display of that char. on the VDU screen and an internal one char. delay, the value of the char address stored in the LP Register will typically be three char. times later than the actual Light Pen location.

2.2.6 VDU Controller Read/Write

When the VDU Controller is addressed, the selected Register is read or written to by a Read or Write operation from the System via the Acorn Bus. The timing of the operations is given on Figure 7. For details of the Register bit significance refer to para 2.2. 1.

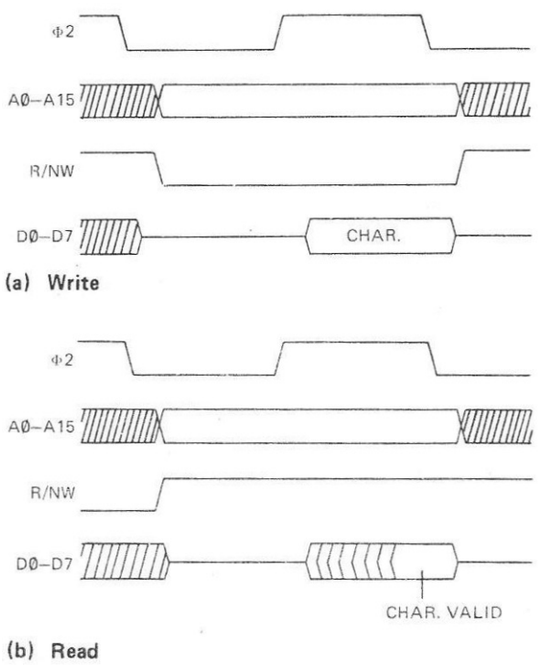

Figure 7. VDU Controller Write and Read

2.2.7 Horizontal Scan

The VDU Controller generates the Character Addresses CA0—CA10 and Raster Addresses RA0-RA3 together with HS and VS signals to produce the composite video output to the VDU.

The CA0—CA10 signals are connected via Multiplexers IC5, IC6 and IC7 to the RAM address inputs. The RA0—RA3 signals are connected directly to the Character Generator ROM IC13. The RA0—RA3 signals are all set to '0' at the beginning of the first scan line of a character row. The CA0—CA10 signals are set to the first character address in the row and then incremented at 2MHz, until the last character address in the row is reached. The Data Enable (DE) signal is set high during this time. Refer to timing diagram, Figure 8.

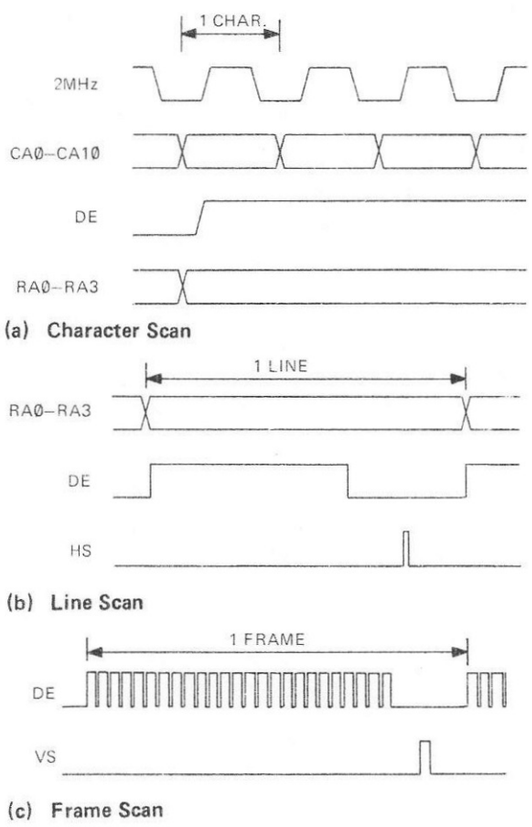

Figure 8. VDU Controller Scan Signals

When the address of the last character to be displayed in the row is reached (specified by the Horiz. Displayed Register), DE is set low. The character address court continues. When the character number in the row, specified as the start of the HS by the HS Position Register, is reached, the HS signal is set high. HS remains high for the number of character times specified in the Sync Width Register.

The character address count continues until the number specified by the Horiz. Total Register plus one is reached. The character number is then reset to the address of the first character in the row, and the scan address is incremented to the next scan line. The horizontal scan process is then repeated for the next scan line and for the other scan lines in the character row.

2.2.8 Vertical Scan

When the last scan line in the character row has been completed, the character address is set to the first character in the next row and the RA0—RA3 signals are all set to '0'. The horizontal scan process is then repeated.

When all the displayed character rows have been scanned, the horizontal scan process is continued for the non-display rows. The VS signal is set high when the row count reaches the value specified in the VS Positions Register. VS remains set high for the number of scan lines specified in the Sync Width Register.

The horizontal scan process continues until the number of character rows specified in the Vert. Total Register plus one have all been scanned. The VDU Controller continues the scan for the number of scan lines specified in the Vert. Total Adjust Register. On completion of the scan of the last line, the scan of one field is completed. The VDU Controller then sets the character address to the address specified in the Start Address Register and starts to scan the next field.

2.2.9 Scan Interface

The VDU Controller can be programmed for non-interlaced or interlaced scan modes. In the non-interlaced mode the VDU Controller produces fields at the programmed rate, e.g. at 50Hz field rate, a field of 312 scan lines can be produced. In the interlaced scan mode alternate odd and even fields are produced to generate frames, e.g. at 50Hz field rate at a frame of 625 scan lines can be produced. The odd fields are displaced by half a scan line time with respect to the even fields, refer to Figure 9. Thus the raster scan of an odd field starts at the centre top of the VDU screen and interlaces between the even field lines previously scanned.

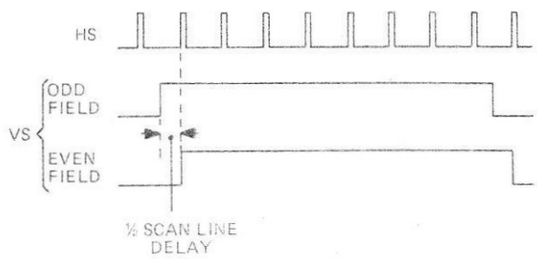

Figure 9. VS Signal Inning Interlace-Sync Mode

2.2.10 Screen Scrolling

To provide the scrolling facility, the VDU Controller counts from the addres in the Start Address Register, to the address determined by the Horiz. Displayed and Vert. Displayed Registers, e.g. 80 char./row by 25 rows = 1999 (7CF hex). The VDU Controller then sets the character address to '0' and counts up to the address in the Start Address Register — 1, to complete the display.

2.3 VDU CLOCK CIRCUIT

The VDU Clock Circuit is used to generate the NL, 2MHz' and 12MHz' clock signals from the Phase 2 (§2) clock input, refer to Figure 10. When 12MHz and 2MHz clock signals are available in the System on the Acorn Bus, the VDU Clock Circuit 2MHz' and 12MHz' Clock Generator Circuits are not used. The Links LK4—LK8 are provided to select the required mode of operation, refer to Table 3.

MODE	Φ2	LINKS
Local Clock Generator	1MHz	LK4, LK7
Local Clock Generator	2MHz	LK5, LK7
External Clocks	—	LK6, LK8

Table 3. VDU Clock Links

The dot Load (NL) clock signal is generated from whichever 2MHz clock source is selected by the Links. The Phase 2 (§2) clock signal is inverted by IC15c to produce the N§2 clock signal irrespective of the selected clock source.

2.3.1 2MHz' Clock Signal Generation

The 2MHz' Oscillator Circuit consists of gates IC16d and IC17b together with associated resistors and capacitors. The §2 clock input is inverted by IC15c to generate N§2. The N§2 clock signal edge is delayed by R 11 and C5, so that exclusive OR gate IC16d generates a short negative pulse, refer to timing diagram Figure 11. The pulse from IC16d synchronizes the 2MHz' Oscillator Circuit IC17b, RV2, R10 and C4. The Oscillator output is connected via LK4 to NAND gate IC18c, which inverts the signal to produce the 2MHz' VDU Clock Circuit output.

When the 2MHz' clock is derived from a 2MHz §2 clock signal, LK5 connects N§2 from IC15c to IC18c to produce the 2MHz' VDU Clock Circuit output.

When the 2MHz clock input is used, LK6 connects the inverted 2MHz output from IC15a to IC18c, to produce the 2MHz' VDU Clock Circuit output.

2.3.2 Load Signal Generation

The Load (NL) signal is generated by IC17d from the selected 2MHz clock signal. R8 and C3 delay the negaedge of the 2MHz clock input to IC18c, so that the positive edge on the output of IC18c is input to IC17d, before C3 discharges below the Schmitt-trigger threshold. A negative pulse, signal NL, of typically 20ns is generated at the output of IC17d at 2MHz frequency.

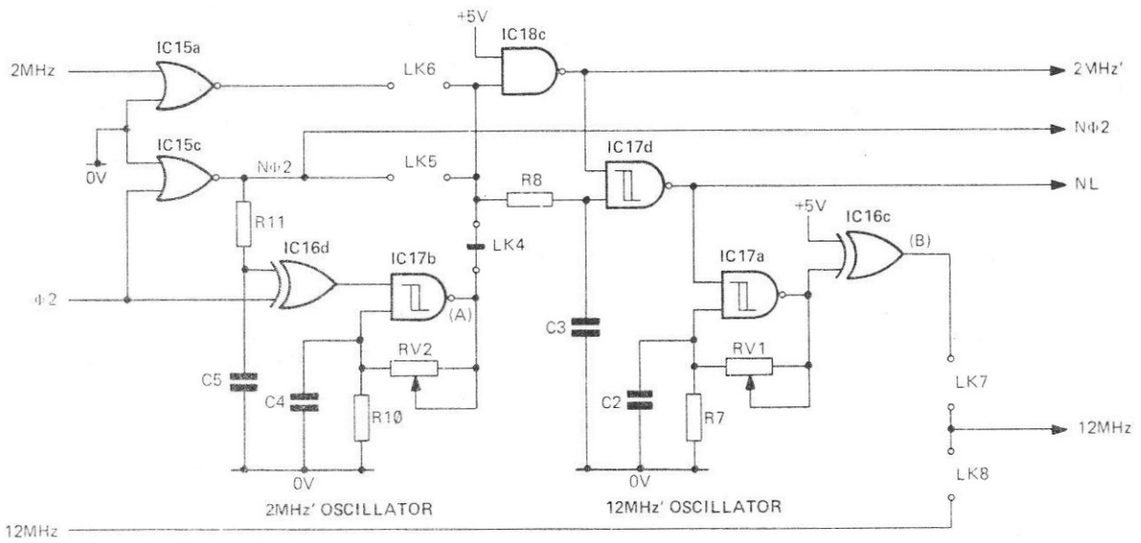

Figure 10. VDU Clock Circuit

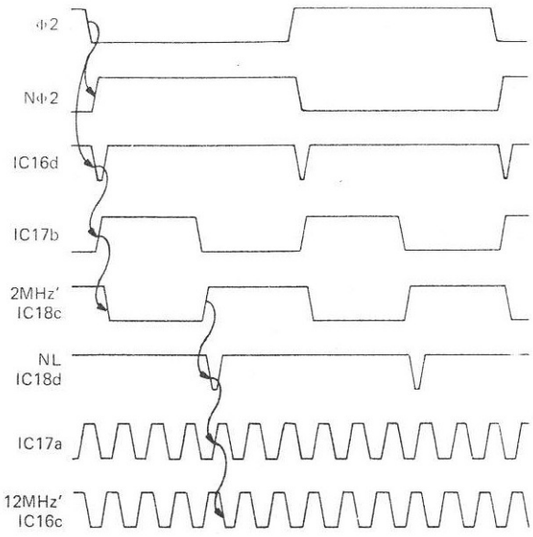

Figure 11. VDU Clock Timing (§2 = 1MHz)

2.3.3 12MHz' Clock Signal Generation

The 12MHz' Oscillator Circuit consists of IC17a, IC16c, RV1, R7 and C2. The NL signal from IC17d synchronizes the 12MHz' Oscillator circuit. The output is connected via inverter IC16c to LK7. When the 12MHz clock from the Acorn Bus is required this is selected by LK8.

2.3.4 VDU Clock Setting-Up Procedure

To set up the VDU Clock Oscillator Circuits the following equipment is required:

Dual-beam oscilloscope
+5V = 1% power supply
Frequency Generator

2MHz` OSCILLATOR
Connect the oscilloscope as follows (refer to Figure 10):

Channel A to IC17/6 (A)
Channel B to §2, IC16/13 (B)

Set the oscilloscope to:

Amplitude	2V/cm
Timebase	100ns/cm
Trigger	Channel B

Connect the +5V supply to the board edge connector as follows:

+5V to Side A pin 1
0V to Side A pin 32

Connect the frequency generator output to the board edge connector Side A pin 29 and 0V to Side A pin 32. Adjust the frequency generator output to 1.00MHz, amplitude +3.5V w.r.t. 0V.

Ensure that the trace on Channel A has the relationship to the §2 signal (Channel B) shown in Figure 11. Adjust RV2 to obtain a symmetrical trace.

12MHz' OSCILLATOR
Connect the oscilloscope Channel A to IC16/8 and ensure that the trace on Channel A is as shown in Figure 11. Adjust RV1 to obtain a symmetrical trace.

2.4 CHARACTER RAM

The Character RAM Circuit consists of the four RAM ICs IC8–IC11, the address Multiplexers IC5, IC6, IC7, the Data Buffer IC4 and the I/O Control Circuit, refer to block diagram Figure 12.

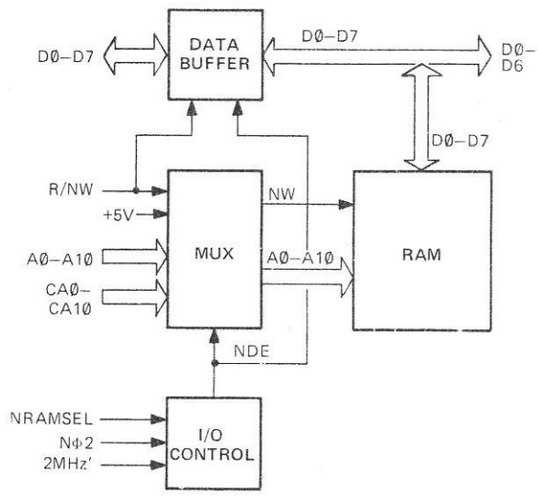

Figure 12. Character RAM Circuit

The D2114 AL-2 RAM ICs are arranged in pairs, each pair provides 1024 (1K) x 8 bit memory locations. The locations are addressed by the Character RAM address lines A0—A10 from the Multiplexers (MUX). The Character RAM Write line (NW) is selected from either the Acorn Bus, R/NW line, or +5V by the MUX.

2.4.1 System Read or Write Operation

The I/O Control Circuit IC15d and IC18b is enabled by a low on the NRAMSEL signal from the Address Selection Circuit, refer to para 2.1.1.

The N§2 clock signal derived from the Acorn Bus Phase 2 (§2) clock signal ie IC15c, is delayed by R14 and C11 and gated with the 2MHz' clock signal from the VDU Clock Circuit at NAND gate IC18b, refer to timing diagram, Figure 13. The Data Enable (NDE)

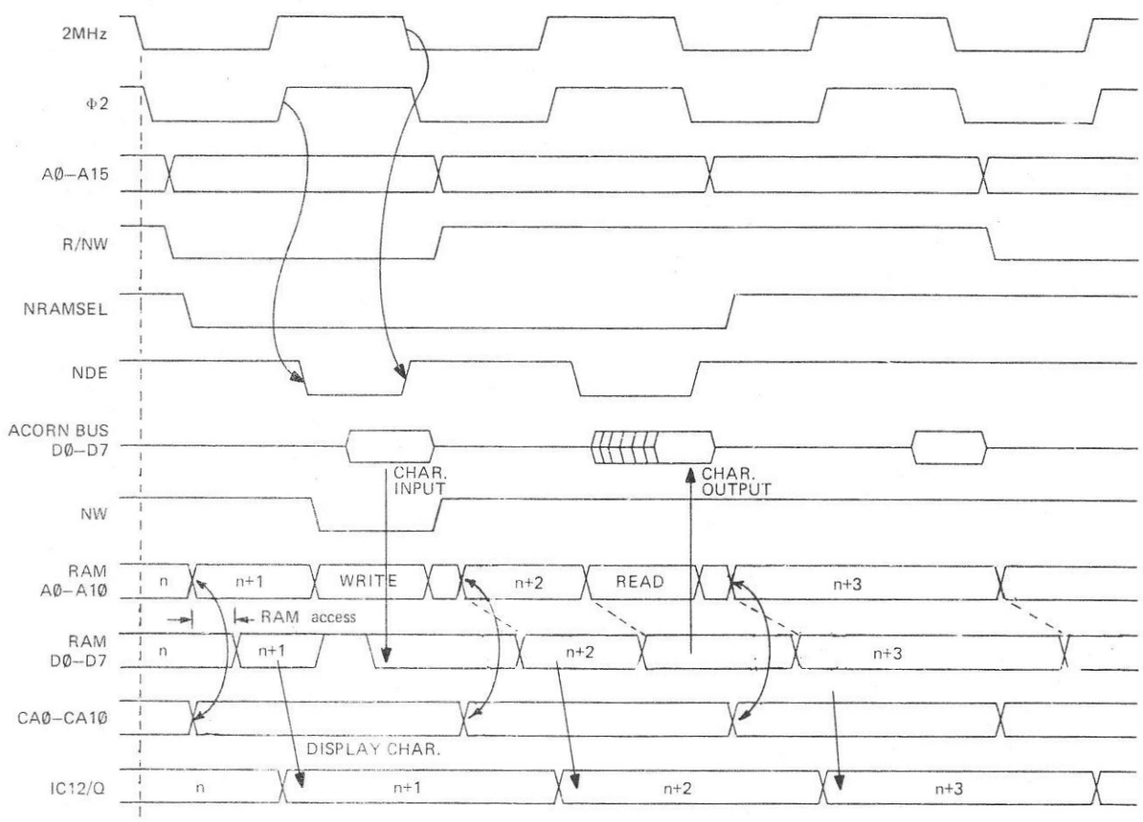

Figure 13. Typical Character RAM Timing

signal from IC18b enables the Data Buffer IC4 for data transfer between the Acorn Bus data lines D0—D7 and the Character RAM data lines D'0—D'7. The direction of transfer is selected by the R/NW signal:

The NDE signal is also used to switch the MUX ICs, to select Acorn Bus address lines A0—A10 as inputs to the Character RAM. The R/NW line is also connected to the Character RAM NW signal line.

For a Write operation the character on D'0—D'7 is written into the Character RAM location addressed by A0—A10 when the NW signal is low.

For a Read operation the character in the location addressed by A0—A10 is output on D'0---D'7.

2.4.2 VDU Controller Read Operation

When the Character RAM is not selected for a System Read or Write operation, the CA0—CA10 address lines from the VDU Controller are connected via the multiplexers to RAM address lines A0—A10. The Character RAM NW line is connected to +5V to inhibit writing to the RAM in this mode of operation.

The character in the location addressed by CA0—CA10, is output onto the data lines D'0—D'7. The Character RAM access time is typically 120ns.

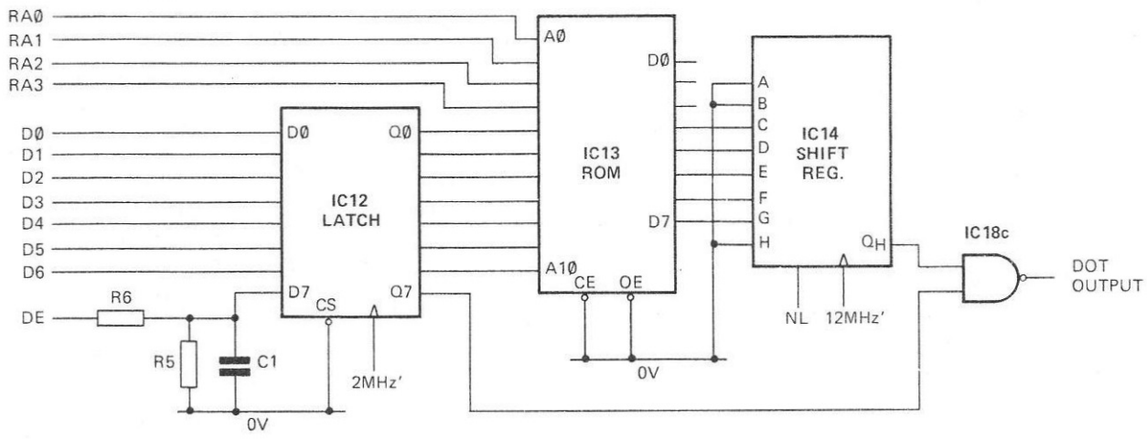

Figure 14. Character Generator Circuit

2.5 CHARACTER GENERATOR

The Character Generator Circuit consists of the octal latch IC12, Programmable ROM IC13 and shift register IC14, refer to Figure 14. Characters stored in the Character RAM are loaded into the octal latch. The latch output addresses the Programmable ROM, which is programmed to decode the character into the appropriate dot pattern for the scan line selected by RA0—RA3. The parallel Character ROM output is converted to a bit serial output by the shift register.

2.5.1 Character Latch

The character code read from the Character RAM on data lines D'0—D'6 (D'7 not connected) is latched into IC12 by the positive edge of the 2MHz' clock signal from the VDU Clock Circuit. In place of the unused D'7 bit signal line, the DE output from the CRT Controller is latched into the eighth bit of IC12. DE is delayed by R5, R6 and C1, so that a change in DE is not latched until one character time after the VDU Controller output changes state.

2.5.2 Character ROM

The RA0—RA3 signals from the VDU Controller determine which is the current scan line in the character row. The character code from the latch IC12 is connected to ROM address inputs A4—A10, so that the programmed dot pattern for a particular character is read from the addressed ROM location onto outputs D3—D7 **(**D0—D2 are not used).

2.5.3 Dot Output

The dot pattern from the ROM is loaded into the shift register IC14 by the NL signal from the VDU Clock Circuit. The dot pattern bits are loaded into the C, D, E, F and G inputs, while '0's are loaded into the A, B and H inputs. The bits in the shift register are then clocked out by the 12MHz` clock signal, starting with bit H. Since the NL signal is generated from the 2MHz' clock only six bits will be shifted out of IC14 before the next NL signal, refer to timing diagram, Figure 15. The next dot pattern is then loaded into IC14.

The QH output of IC14 is connected to NAND gate IC18d. The delayed DE signal latched in IC12, enables IC18d, when a character is to be displayed. The character dots are then inverted by IC18d, so that a '0' represents a dot and a '1' a space on the VDU screen. This output is connected to the Video Output Circuit.

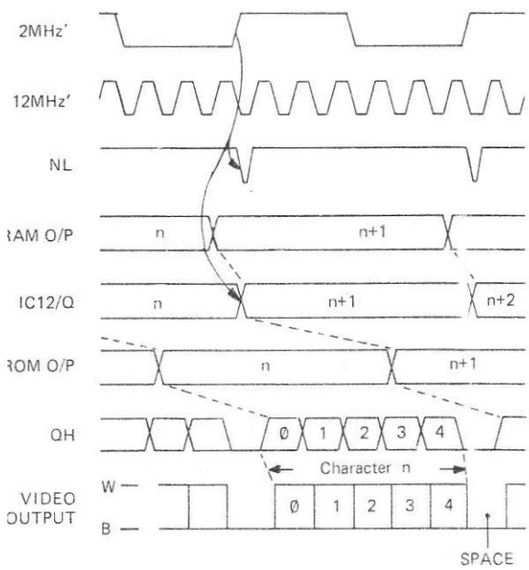

Figure 15. Character Generator Timing

2.6 VIDEO OUTPUT

The Video Output Circuit translates the binary dot pattern from the Character Generator into the analogue video output, refer to Figure 16. The circuit also mixes in the HS, VS and Cursor signals to provide the composite video for the VDU, refer to Figure 17.

2.6.1 Dot Display

When characters are to be displayed, signal DE from the VDU Controller is high enabling dot output, refer to para 2.5.1. The CU signal from the VDU Controller is low except for the character time when the Cursor is displayed. Link LK2 is open circuit for the display of white characters on a black background. These conditions produce a high output from exclusive OR gate IC16a, so that a dot bit low on the dot output from the Character Generator produces a high at the output of exclusive OR gate IC16/6. The output transistor TR1 is turned on by the high on IC16/6 to supply +1V on the VDU connector pin 1. When the dot bit output is high (no display dot), IC16/6 goes low. The low on IC16/6 pulls down the voltage on TR1 base, but diodes D2, D3 and D4 limit the voltage excursion. TR1 then supplies the black level output voltage of +0.3V approximately on the VDU connector pin 1.

2.6.2 Cursor Display

The VDU Controller may be programmed for either Block or Underline Cursor displayr For Block Cursor the CU signal is high for all scan lines during the selected character time. For Underline Cursor the CU signal is high for the selected number of scan lines during the selected character time. The CU signal can be delayed by one or two character times under program control, to allow for RAM access delay.

The CU signal high is delayed by R12, R13 and C6 to allow for dot signal propagation times. The CU signal high at IC16/1 and the +5V via R9 at IC16/2 generate a low output from the exclusive OR gate or IC16/3. This low at IC16/4 inverts the dot output. In Block Cursor mode the character displayed during the Cursor time will appear as black on a white background. In Underline Cursor mode the character position will he underlined by a solid bar.

2.6.3 Sync Signals

When the HS or VS signals are high IC15/4 output goes low. This low pulls down the voltage on the base of TR1 via diode D1 to turn off the transistor. When TR1 is off the voltage output on the VDU connector pin 1 falls to 0V, the video signal sync level.

2.6.4 Display Inversion

Link LK2 is provided to allow display inversior when required. Connecting a link in the LK2 position connects 0V to IC16/2. The output on IC16/3 is then low except when the CU signal from the VDU Controller is high. The dot output will generate a black level signal for a dot or a white level for spaces. The display on the VDU screen will consist of black dots on a white background. The Block Cursor will also be inverted to produce white dots on a black block.

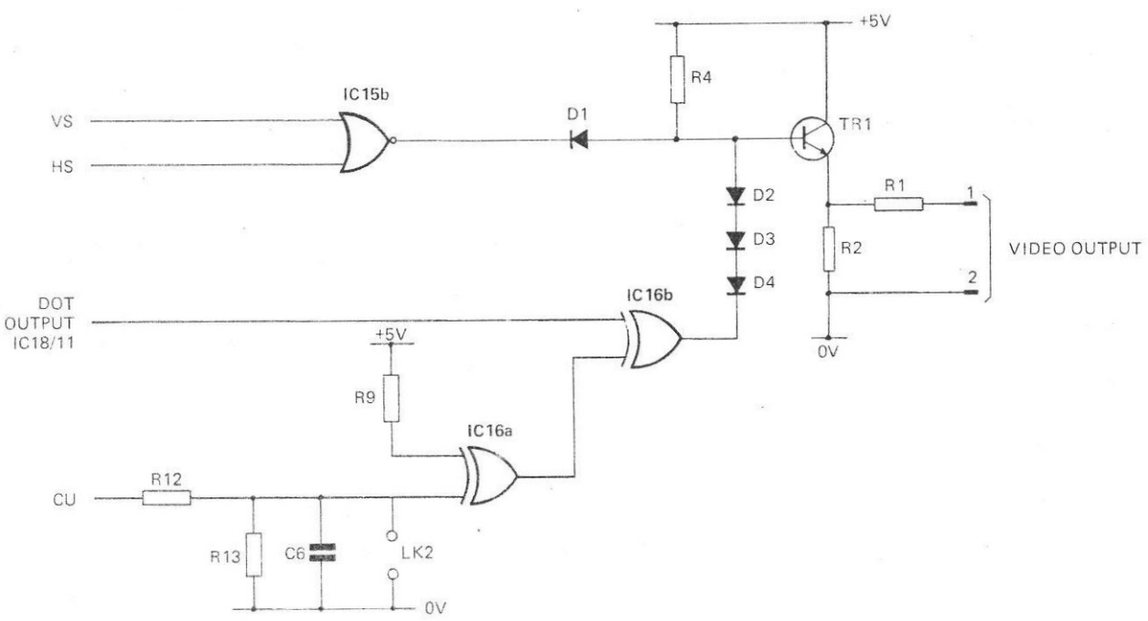

Figure 16. Video Output Circuit

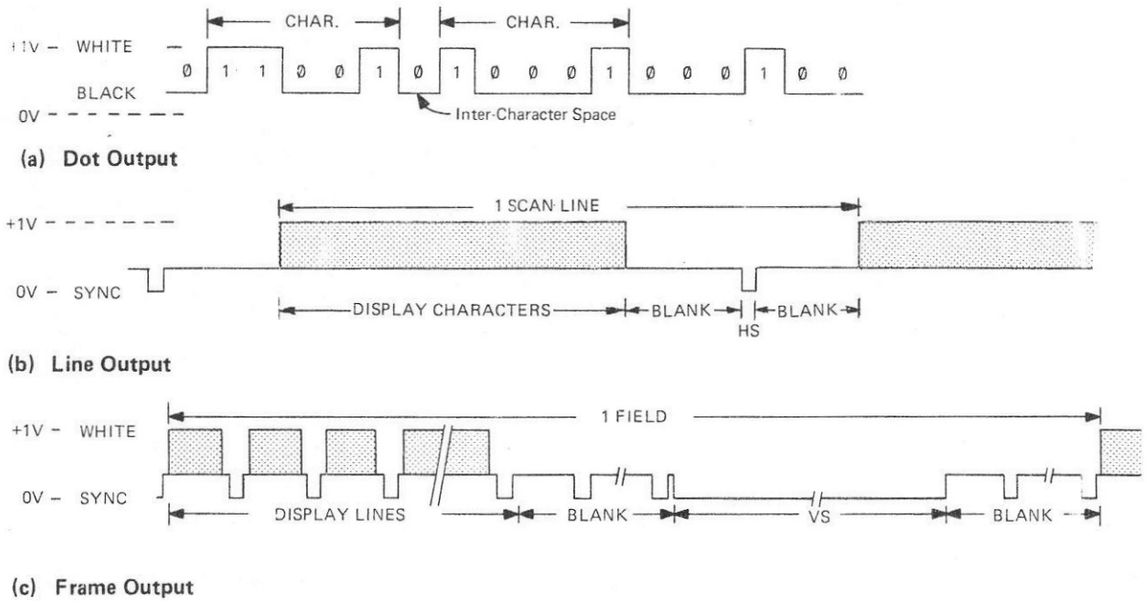

Figure 17. Composite Video Output Signal

3. SOFTWARE PARAMETERS

3.1 VDU LNTERFACE ADDRESSING

The Acorn Bus address lines A11—A15 are decoded for the Character Ram and VDU Controller addresses.

3.1.1 Character RAM

The Character RAM can be located at one of two locations by links on the VDU Board. Links LK7—LK10 in the A position select RAM addresses 1000—17FF (hex). In the B position addresses F000—F7FF (hex) are selected.

3.1.2 VDU Controller

The VDU Controller is normally assigned addresses 1840 and 1841 (hex), Links LK7—LK10 in the A position. Since the address lines are not completely decoded, the addreses 1840-187F (hex) must be assigned to the VDU Controller. In the B position addresses E840—E87F (hex) are assigned to the VDU Controller.

3.1.3 Paging Facility

The VDU Board is provided with a paging facility. The Board is supplied with a track link in LK3, to use the facility the link must be cut. The Valid Memory Address (NVMA) signal input on the Acorn Bus con nector pin 24b, will then select the VDU Board when ' 0'.

3.2 VDU CONTROLLER

The VDU Controller is provided with internal programmable Registers. The Registers are listed in Table 2, and described in para 2.2.1.

3.2.1 Register Addressing

The Address Register is addressed when the A0 address bit is '0'. To select the required Control Register, the Register number is loaded into the Address Register from data bits D0—D4 by a Write operation. Subsequent Read or Write operations to the VDU Controller with A0 = '1' will then be vectored to the required Control Register.

3.2.2 Mode Control

The VDU Controller Interlace and Skew Register (R8) selects the mode of operation required as follows (bits 2 and 3 are not used):

INTERLACE MODE CONTROL
Bits 1 and 0 select the VDU scan interlace required.

- Non-interlaced Mode (bit 0 = '0') provides a non-interlaced scan, e.g. 312 lines at 50Hz.
- Interlaced Sync Mode (01), is used to enhance readability of characters. The same information is displayed in odd and even fields to produce a higher quality character display. The scan is interlaced so that each frame is two complete fields, e.gr a 50Hz 625 line frame will comprise two fields of 312½ lines superimposed, refer to para 2.2.9.
- interlaced Sync and Video Mode (11) not used:

CURSOR SKEW
Bits 5 and 4 select cursor operation and the amount of cursor skew as follows:

- Non-skew (00). Cursor operation selected with no skew delay.

  One char, skew (01). Cursor operation selected with a skew of one char. time.

- Two char. skew (10). Cursor operation selected with a skew of two char. times.

  No Cursor (11). Cursor operation not selected.

DISPLAY ENABLE SKEW
Bits 7 and 6 select Display Enable (DE) signal output and the amount of skew as follows:

- Non-skew (00). Display enabled with no skew.
- One charr skew (01). Display enabled after a delay of one char. time.
- Two char, skew (10). Display enabled after a delay of two char. times.
- No Display (11). DE signal output inhibited.

3.2.3 Display Configuration

The Register settings used in System 5 to program the VDU Controller for operation at 50Hz field rate with non-interlaced scan (312 lines+field) are given in Table 4.

REGISTER	CODE (HEX)	SIGNIFICANCE
R0	7F	123 char./row
R1	50	80 char. displayed/row
R2	66	HS starts at char. 102 VS = 6 lines scan time
R3	62	HS = 2 char. times
R4	1E	31 rows/field
R5	02	2 additional lines/field
R6	19	25 rows displayed/field
R7	18	VS starts at row 27
R8	40	Mode selected: — Non-interlace — 1 charr Cursor delay — No Display Enable delay
R9	09	10 scan lines/charr row
R10	68	Cursor blink at 1/32 field rate Cursor start: line 8
R11	09	Cursor end: line 9
R12 R13	10 00	Display start address char. 0000 (RI2 bit 4 not used by VDU Controller).

Table 4. Register Settings

4. 80 x 25 VDU INTERFACE BOARD CONNECTIONS

4.1 VDU BOARD TO ACORN BUS

Pin	Mnemonic	Meaning	I/O
Side A			
1	+5V	+5V Supply	I
2	A15	Address Lines	I
3	A14		
7	A8		
8	A7		
9	A6		
10	A5		
11	A4		
12	A3		
13	A2		
14	A1		
15	A0		
16	D7	Data Lines	I/O
17	D6		
18	D5		
19	D4		
20	D3		
21	D2		
22	D1		
23	D0		
24	A13	Address Lines	I
25	A12		
26	A11		
27	A10		
28	A9		
29	Φ2	Phase Two Clock	I
30	R/NW	Read/Write	I
32	0V	0V Supply	I
Side B			
13	12MHz	System Clocks	I
18	2MHz		
24	NVMA	Valid Memory Address	I
32	0V	0V Supply	I

4.2 VDU BOARD TO VDU

Pin	Mnemonic	Meaning	I/O
1		Video Output	O
2		Video Output (0V)	O
3		+5V Supply	O
4		Light Pen	I
5		Light Pen (0V)	O

5: PARTS LIST

5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
	PCB 200, 019 issue 1		1	
	24 pin IC Socket		1	
	20 pin IC Socket		3	
	18 pin IC Socket		4	
	16 pin IC Socket		6	
	14 pin IC Socket		4	

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NC.
C1	Capacitor	330pF	1	
C2	Capacitor	47pF	1	
C3	Capacitor	150pF	1	
C4, C5	Capacitor	470pF	2	
C6	Capacitor	330pF	1	
C7...C9	Capacitor	47nF	3	
C10	Capacitor, electrolytic	10µF 25V	1	
C11	Capacitor	150pF	1	
	Connector 64-way Plug (Right angle solder tails to DIN 41612)		1	
D1...D4	Diode	IN4148	4	
IC1, IC2	Integrated Circuit	74LS138	2	
IC3	Integrated Circuit	HD46505SP-2	1	
IC4	Integrated Circuit	8208	1	
IC5...IC7	Integrated Circuit	74LS157	3	
IC8...IC11	Integrated Circuit	2114-2	4	
IC12	Integrated Circuit	74LS374	1	
IC13	Integrated Circuit	MM52116 F DW*	1	
IC14	Integrated Circuit	74LS165	1	
IC15	Integrated Circuit	74LS02	1	
IC16	Integrated Circuit	74LS86	1	
IC17	Integrated Circuit	74LS132	1	
IC18	Integrated Circuit	74LS00	1	
RV1, RV2	Potentiometer, Miniature Skeleton	1kOhm	2	
R1	Resistor Carbon	47Ohm 0.25W	1	
R2	Resistor Carbon	100Ohm 0.25W	1	
R3	Resistor Carbon	47kOhm 0.25W	1	
R4	Resistor Carbon	1kOhm 0.25W	1	
R5	Resistor Carbon	4.7kOhm 0.25W	1	
R6	Resistor Carbon	3.3kOhm 0.25W	1	
R7	Resistor Carbon	1kOhm 0.25W	1	
R8	Resistor Carbon	150Ohm 0.25W	1	
R9	Resistor Carbon	10kOhm 0.25W		
R10	Resistor Carbon	1.2kOhm 0.25W		
R11	Resistor Carbon	82Ohm 0.25W	1	

*Programmed by Acorn.

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
R12	Resistor Carbon	1kOhm 0.25W	1	
R13	Resistor Carbon	2.7kOhm 0.25W	1	
R14	Resistor Carbon	82Ohm 0.25W	1	
TR1	Transistor	2N2369	1	

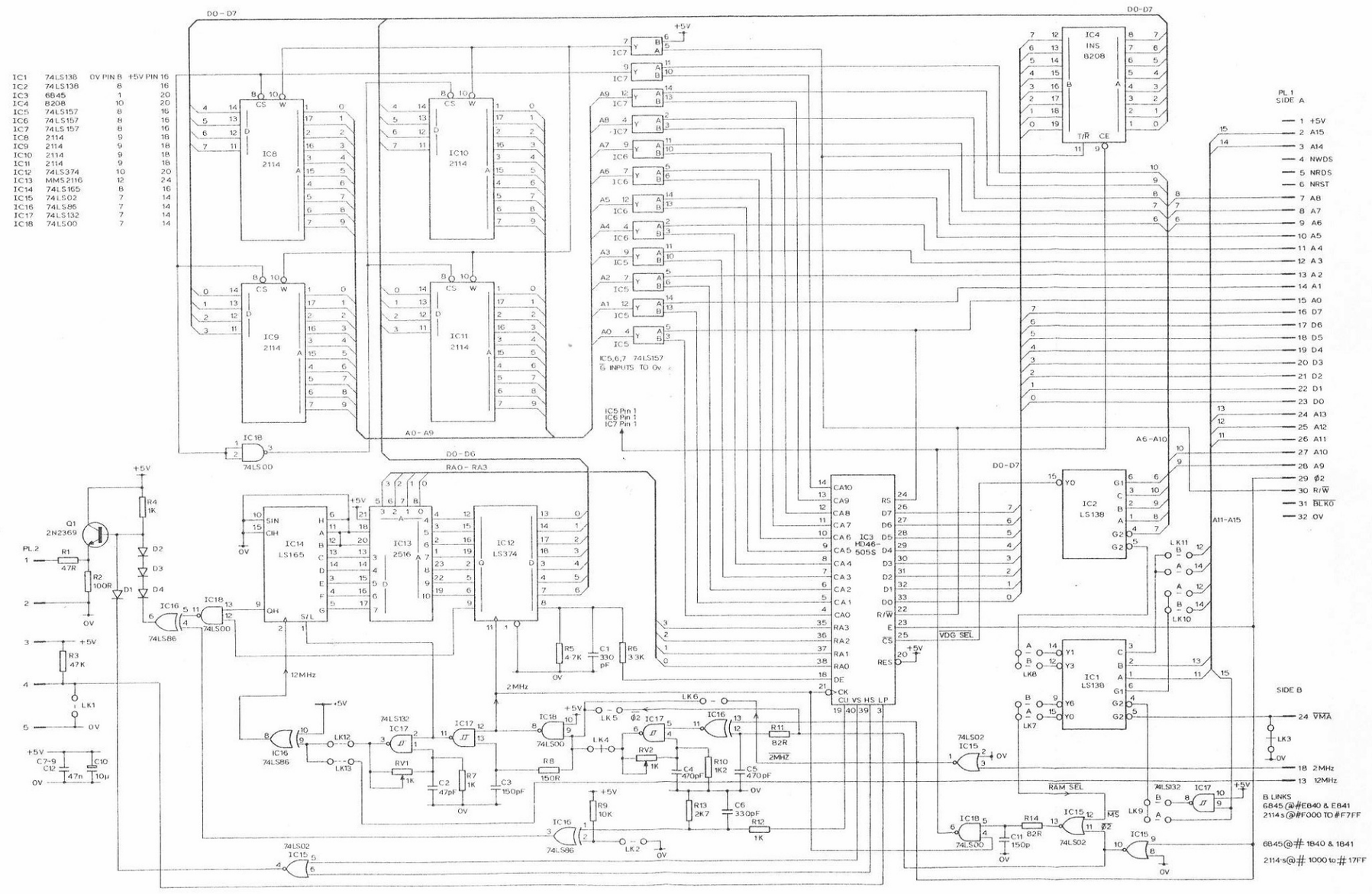

Figure 18. 80 x 25 VDU Interface Circuit Diagram